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10/750,150	12/31/2003	Gary N. Hammond	42P18219	7903

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,150	HAMMOND ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003 and 14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181

4/4/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 12/31/2003, Declaration on 06/14/2004, and Status Inquiry on 09/06/2005.

Claim Objections

3. Claims 11-13 are objected to because of the following informalities: Regarding claim 11, the word "store" in the limitation "instruction scheduler to *store* track only store instructions" should be removed as it appears to be a typographical error.

4. All claims objected to that have not been specifically addressed above are objected to on the basis of dependence.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 14 recites the limitation "means for tracking all instructions in program order coupled to the means for tracking only speculative instructions" in lines 3-4 of the claim. There is insufficient antecedent basis for this limitation in the claim since there is

no previous mention of a "means for tracking only speculative instructions". However, since there is mention of a "means for tracking only speculative *load* instructions" (See line 2 of claim), the recited limitation "means for tracking all instructions in program order coupled to the means for tracking only speculative instructions" will be interpreted as "means for tracking all instructions in program order coupled to the means for tracking only speculative load instructions" for the remainder of the examination.

8. All claims rejected by 35 U.S.C. 112, second paragraph, that have not been specifically addressed above are rejected on the basis of dependence.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-3, 5-7, 14, 17, and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Morris et al., U.S. Patent Application Publication No. 2004/0168045 (Herein referred to as Morris).

11. Referring to claim 1, Morris has taught a method comprising:

issuing a load instruction to an execution cluster *[execution unit; Fig. 1; component 20]* in an out of order processor *[See paragraphs 22-24]*; and

allocating an entry for the load instruction in a structure *[speculative-load-instruction manager (SLIM); Fig. 1, component 29]* for tracking only load instructions only if the load instruction utilizes speculative data *[See paragraph 15]*.

12. Referring to claim 2, Morris has taught the method of claim 1, further comprising:

indicating the load instruction that uses speculative data is to be checked at retirement *[By entering a load instruction into the SLIM, it is indicated that the instruction is to considered further (i.e. checked) at retirement of the corresponding check instruction; See paragraphs 29 and 32]*; and

searching the structure for tracking only load instructions for the entry for the load instruction to confirm the load data at the time of retirement *[At retirement a check instruction finds the corresponding s-load instruction (i.e. searches the SLIM) and determines whether or not the corresponding s-load instruction has been rendered invalid (i.e. the load data is confirmed); See paragraph 32]*.

13. Referring to claim 3, Morris has taught the method of claim 1, further comprising:

invalidating the entry for the load instruction during a store instruction retirement if the store instruction conflicts with the load instruction *[If the s-load syndrome matches that broadcast by a store instruction (i.e. a store instruction conflicts with the load instruction) the s-load is marked invalid in the SLIM; See paragraph 30]*.

14. Referring to claim 5, Morris has taught the method of claim 1, wherein the load instruction is an advanced load instruction *[The load instruction has been advanced in front of a store instruction; See paragraph 5]*.

15. Referring to claim 6, Morris has taught the method of claim 5, further comprising: converting a basic load instruction into an advanced load instruction *[See paragraph 12]*.

16. Referring to claim 7, Morris has taught the method of claim 1, wherein the structure for tracking load instructions is an advanced load allocation table *[The SLIM is a table that allocates entries for speculative advanced load instructions and is, therefore, an advanced load allocation table; See paragraph 15]*.

17. Referring to claim 14, Morris has taught an apparatus comprising:

means for tracking only speculative load instructions *[speculative-load-instruction manager (SLIM); Fig. 1, component 29; See paragraph 15]*; and

means for tracking all instructions in program order *[instruction queue; Fig. 1, component 25; See paragraph 23]* coupled to the means for tracking only speculative load instructions, comprising a field to indicate a load instruction is to be checked at retirement *[A speculative load instruction has a corresponding load check instruction, which is stored in an instruction queue field and indicates that the load instruction is to be checked at retirement; See paragraph 15]*.

18. Referring to claim 17, Morris has taught a machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

tracking only a set of load instructions relying on speculative data in a first data structure of an out of order processor *[speculative-load-instruction manager (SLIM); Fig. 1, component 29; See paragraph 15]*; and

tracking a set of instructions in program order in a second data structure *[instruction queue; Fig. 1, component 25; See paragraph 23]* having a field to indicate to check speculation in a load instruction at a time of load instruction retirement *[A speculative load instruction has a corresponding load check instruction, which is stored in an instruction queue field and indicates that the load instruction is to be checked at retirement; See paragraph 15].*

19. Referring to claim 19, Morris has taught the machine readable medium of claim 17, having instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

invalidating allocated load instruction entries during store instruction retirement *[If the s-load syndrome matches that broadcast by a store instruction the s-load is marked invalid (i.e. the load entry is invalidated) in the SLIM; See paragraph 30].*

20. Referring to claim 20, Morris has taught the machine readable medium of claim 17, wherein the first data structure is an advanced load allocation table *[The SLIM is a table that allocates entries for speculative advanced load instructions and is, therefore, an advanced load allocation table; See paragraph 15].*

21. Referring to claim 21, Morris has taught the machine readable medium of claim 17, wherein the second data structure is a reorder buffer *[The instruction queue retires*

instructions in order (i.e. reorders the instructions) and, therefore, it is a reorder buffer; See paragraph 23].

22. Claims 8 and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by McNairy et al., "Itanium 2 Processor Microarchitecture" (Herein referred to as McNairy).

23. Referring to claim 8, McNairy has taught a device comprising:

a store queue *[store buffer; See Fig. 4]* in an out of order processor to track only store instructions *[page 52, 2nd column, 1st paragraph]*; and

a load queue *[ALAT; See Fig. 1]* coupled to the store queue to track only speculative load instructions *[page 51, 2nd column, last paragraph].*

24. Referring to claim 10, McNairy has taught the device of claim 8, wherein the load queue is an advanced load allocation table *[page 51, 2nd column, last paragraph].*

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 9, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McNairy in view of Johnson, "Superscalar Microprocessor Design".

27. Referring to claim 9,

McNairy has taught the device of claim 8, further comprising:

an instruction scheduler *[instruction decode and dispersal unit; See Fig. 1]* coupled to the store queue to schedule instruction execution *[The dispersal logic assigns instructions to execution units (i.e. schedules their execution); See 3rd paragraph of the section labeled "Instruction dispersal", which starts on page 48]*; and

McNairy has not explicitly taught a reorder buffer coupled to the instruction scheduler to track program order of instructions and to track speculative load instructions to be checked at retirement.

Johnson has taught a reorder buffer *[See section 5.1.4 on pages 92-94]* coupled to the instruction scheduler to track program order of instructions and to track speculative load instructions to be checked at retirement *[The reorder buffer tracks all instructions, including load instructions that are to be checked at retirement; See 1st full paragraph on page 93]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the device of McNairy to include a reorder buffer coupled to the instruction scheduler to track program order of instructions and to track speculative load instructions to be checked at retirement as taught by Johnson.

The suggestion/motivation for doing so would have been that doing so simplifies the maintenance of the instruction order *[See 1st paragraph of section labeled "Using a Reorder Buffer to Simplify the Central Window" on page 139]*.

Therefore, it would have been obvious to combine Johnson with McNairy to obtain the invention as specified in claim 9.

28. Referring to claim 11,

McNairy has taught a system comprising:

a first processor *[Itanium 2 processor; See Fig. 1]* having at least a 64 bit architecture *[See 1st paragraph of section labeled "Microarchitecture overview" on page 44]* comprising

a first data cache *[L1D cache; See Fig. 1]*,

set of execution units *[Integer ALUs; See Fig. 1]*,

instruction scheduler *[Instruction decode and dispersal unit; See Fig. 1; See section labeled "Instruction dispersal" starting on page 48]* coupled to the data cache and set of execution units,

a store queue *[store buffer; See Fig. 4]* coupled to the instruction scheduler to track only store instructions *[See page 52, 2nd column, 1st paragraph]* and

a load queue *[ALAT; See Fig. 1]* coupled to the store queue to track only speculative load instructions *[See page 51, 2nd column, last paragraph]*;

a bus coupled to the processor *[System interface bus; See Fig. 4]*; and

a system memory device *[system memory; See 3rd paragraph under subsection labeled "System interface"]* coupled to the bus.

McNairy has not explicitly taught that the instruction scheduler is an out of order instruction scheduler.

Johnson has taught out of order instruction issuing (i.e. scheduling) *[1st and 2nd paragraphs on page 21].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the instruction scheduler of McNairy to schedule instruction out of order as taught by Johnson.

The suggestion/motivation for doing so would have been that doing so "gives the processor a larger set of instructions available for issue, improving its chances of finding instructions to execute concurrently" *[See 1st full paragraph on page 22].*

Therefore, it would have been obvious to combine with McNairy to obtain the invention as specified in claim 11.

29. Referring to claim 13,

McNairy and Johnson have taught the system of claim 11.

McNairy and Johnson have not explicitly taught a reorder buffer to track program order of instructions and to track speculative load instructions to be checked at retirement.

Johnson has taught a reorder buffer *[See section 5.1.4 on pages 92-94]* to track program order of instructions and to track speculative load instructions to be checked at retirement *[The reorder buffer tracks all instructions, including load instructions that are to be checked at retirement; See 1st full paragraph on page 93].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of McNairy and Johnson to include a

reorder buffer to track program order of instructions and to track speculative load instructions to be checked at retirement as taught by Johnson.

The suggestion/motivation for doing so would have been that doing so simplifies the maintenance of the instruction order *[See 1st paragraph of section labeled "Using a Reorder Buffer to Simplify the Central Window" on page 139].*

Therefore, it would have been obvious to combine Johnson with McNairy and Johnson to obtain the invention as specified in claim 13.

30. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over McNairy and Johnson, as applied to claim 11 above, and further in view of Hennessy et al., "Computer Architecture: A Quantitative Approach" (Herein referred to as Hennessy).

31. Referring to claim 12,

McNairy and Johnson have taught the system of claim 11.

McNairy and Johnson have not explicitly taught a second processor coupled to the bus comprising a second data cache.

Hennessy has taught a second processor coupled to a bus comprising a second data cache *[See Fig. 6.1 on page 531].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of McNairy and Johnson to include a second processor coupled to a bus comprising a second data cache as taught by Hennessy.

The suggestion/motivation for doing so would have been that doing so improves performance of the processing system *[See 2nd paragraph on page 528]*.

Therefore, it would have been obvious to combine Hennessy with McNairy and Johnson to obtain the invention as specified in claim 12.

32. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Arora, U.S. Patent No. 6,598,156.

33. Referring to claim 4,

Morris has taught the method of claim 2, further comprising:

correcting for erroneous speculation if the structure for tracking only load instructions does not contain a valid entry for the load instruction at load instruction retirement *[See paragraph 32]*.

Morris has not explicitly taught that the correcting for erroneous speculation includes flushing a pipeline.

Arora has taught flushing a pipeline to correct for erroneous speculation *[See Fig. 3, component 350; column 6, lines 26-31, 57-62]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the correction for erroneous speculation as taught by Morris to include flushing a pipeline as taught by Arora.

The suggestion/motivation for doing so would have been that doing so would prevent dependent instructions from using stale data *[See column 6, lines 47-62]*.

Therefore, it would have been obvious to combine Arora with Morris to obtain the invention as specified in claim 4.

34. Referring to claim 16,

Morris has taught the apparatus of claim 14, further comprising:

means for correcting erroneous speculation upon detection that a speculative load is not present in the means for tracking only speculative loads at the time of load instruction retirement *[See paragraph 32]*.

Morris has not explicitly taught that the correcting for erroneous speculation includes flushing a pipeline.

Arora has taught flushing a pipeline to correct for erroneous speculation *[See Fig. 3, component 350; column 6, lines 26-31, 57-62]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the correction for erroneous speculation as taught by Morris to include flushing a pipeline as taught by Arora.

The suggestion/motivation for doing so would have been that doing so would prevent dependent instructions from using stale data *[See column 6, lines 47-62]*.

Therefore, it would have been obvious to combine Arora with Morris to obtain the invention as specified in claim 16.

35. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris in view of Johnson.

36. Referring to claim 15,

Morris has taught the apparatus of claim 14.

Morris has not explicitly taught a means for tracking only store instructions coupled to means for tracking only speculative load instructions.

Johnson has taught a means for tracking only store instructions *[store buffer; page 51, 1st full paragraph]* coupled to means for tracking only speculative load instructions *[The store buffer is part of the processor and, therefore, coupled to all of the processors components including the means for tracking only speculative load instructions]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the apparatus of Morris to include a means for tracking only store instructions coupled to means for tracking only speculative load instructions as taught by Johnson.

The suggestion/motivation for doing so would have been that doing so preserves the processor's in-order state *[page 51, 1st full paragraph]*.

Therefore, it would have been obvious to combine Johnson with Morris to obtain the invention as specified in claim 15.

37. Referring to claim 18,

Morris has taught the machine readable medium of claim 17, having instructions stored therein which when executed causes a machine to perform a set of operations.

Morris has not explicitly taught tracking only a set of store instructions in a store queue of the out of order processor.

Johnson has taught tracking only a set of store instructions in a store queue *[store buffer; page 51, 1st full paragraph]* of the out of order processor.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Morris to include tracking only a set of store instructions in a store queue of the out of order processor as taught by Johnson.

The suggestion/motivation for doing so would have been that doing so preserves the processor's in-order state *[page 51, 1st full paragraph]*.

Therefore, it would have been obvious to combine Johnson with Morris to obtain the invention as specified in claim 18.

Conclusion

38. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arora et al., U.S. Patent No. 6,658,559, teaches a system for executing advanced load instructions.

Miyake et al., U.S. Patent No. 6,998,315, teaches a system for executing speculative load instructions.

Franklin et al., "ARB: A Hardware Mechanism for Dynamic Reordering of Memory References", teaches a system for dynamically disambiguating memory references.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
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4/2/2006